1449A/PTO Rev. 10/95	U.S. Department of Commerce Patent and Trademark Office	Complete If Known	
LIST OF PRIOR ART CITED BY APPLICANT *(use as many sheets as necessary)*		Application Number	
		Filing Date	03-23-04
		First Named Inventor	Douglas James Tweet
		Group Art Unit	
		Examiner Name	
Sheet 1 of 1		Attorney Docket No.	SLA.0586

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, country where published, source.	T[2]
WLL		HARRISON *ET AL.*, *Highly performant double gate MOSFET realized with SON process*, IEDM 03-449, p18.6.1 (2003)	
WLL		YIN, *ET AL.*, *Strain relaxation of SiGe islands on compliant oxides*, J. Appl. Phys. 91, p. 9716 (2002).	
WLL		R. CHAU *ET AL.*, *A 50nm Depleted-Substrate CMOS Transistor*, IEDM, p. 621, 2001.	
WLL		TEZUKA *ET AL.*, *A Novel Fabrication Technique of Ultrathin and Relaxed SiGe Buffer Layers with High Ge Fraction for Sub-100nm Strained Silicon-on-Insulator MOSFETs*, Jpn. J. Appl. Phys. 40, p. 2866 (2001)	
WLL		M. JURCZAK, *ET AL.*, *Silicon-on-Nothing (SON) - an innovative Process for Advanced CMOS*, IEEE Trans. El. Dev. Vol. 47, pp2179-2187 (2000).	
WLL		MIZUNO *ET AL.*, *Advanced SOI-MOSFETs with strained-Si channel for high speed CMOS - electron/hole mobility enhancements*, 2000 Symposium on VLSI, p. 210.	
WLL		TRINKAUS *ET AL.*, *Strain relaxation mechanism for hydrogen-implanted $Si_{1-x}Ge_x/Si$ (100) heterostructures*, Appl. Phys. Lett., 76, p. 3552, (2000).	
WLL		M. JURCZAK *ET AL.*, *SON (Silicon on Nothing) - A New Device Architecture for the ULSI Era*, VLSI Tech. Dig., p.29, (1999).	
WLL		R. KOH, *Buried Layer Engineering to Reduce the Drain-Induced Barrier Lowering of Sub-0.05um SOI-MOSFET* Jpn. J. Appl. Phys., Vol. 38, P. 2294 (1999)	
WLL		MANTL *ET AL.*, *Strain relaxation of epitaxial SiGe layers on Si (100) improved by hydrogen implantation*, Nuclear Instruments and Methods in Physics Research B 147, p. 29, (1999)	
WLL		PAUL, *Silicon germanium heterostructures in electronics: the present and the future*, Thin Solid Films, 321, p. 172 (1998)	
WLL		RIM *ET AL.*, *Transconductance enhancement in deep submicron strained-Si n-MOSFETs*, IEDM Proc. p. 707 (1998)	
WLL		WELSER *ET AL.*, *Electron mobility enhancement in strained-Si N-type metal-oxide-semiconductor field-effect transistors*, IEEE EDL-15, #3, p.100, (1994)	
WLL		RIM *ET AL.*, *Enhanced hole mobilities in surface-channel strained-Si p-MOSFETs*, IEDM Proc. p. 517 (1995)	

Examiner Signature	Walter L. Lindsay Jr.	Date Considered	6/2/2005

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